IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 9216

Arthur Ray Alexander

Group Art Unit: 2827

Serial No.: 09/752,352

Examiner: I.B. Patel

Filed: 12/29/2000

For: INTRODUCING LOSS IN A POWER BUS TO REDUCE EMI AND ELECTRICAL NOISE

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

This is a reply to the office action dated August 14, 2002, in this application. Claims 1-3, 5-8, 17, 19 and 20 are pending. Please amend claim 20 as follows.

20. (Amended) A printed circuit board comprising multiple layers, including:

at least one layer on which electronic circuitry resides;

at least one power layer for use in providing electric current to the electronic circuitry, comprising:

at least one resistive element formed in a void in the power layer and connected electrically to the power layer to suppress electrical noise created by sudden changes in current flow; and

at least one capacitive element connected in series with the resistive element.

REMARKS

Claims 1-3, 5-8, 17, 19 and 20 are pending in this application. The Office has rejected claim 20 under 35 U.S.C. § 112 as being indefinite. Claims 1, 2, 6, 17 and 20 were rejected under 35 U.S.C. § 102(e) in view of Archambeault. Claims 7, 8 and 19 were rejected under 35 U.S.C. § 103(a) in view of Archambeault and Klaser, and claims 3 and 5 were rejected in view of Archambeault, Ehman and Nakanishi.

Applicant has amended claim 20 and asks the Examiner to reconsider this application and allow all of the claims.

Improper Final Action

The action of August 4 is an improper final action. Applicant asks that the action be withdrawn and that a new, non-final action be issued in its place.

MPEP 706.07(a) states that, "a second or any subsequent action on the merits in any application . . . will not be made final if it includes a rejection, on newly cited art . . . of any claim not amended by applicant . . . in spite of the fact that other claims may have been amended to require newly cited art." The Office asserts that Applicant's amendments to claims 1 and 17 necessitated the new ground of rejection, but this simply is not true.

In amending claims 1 and 17, Applicant did nothing more than move the limitations of dependent claims 4 and 18 into the independent claims. In other words, current claims 1 and 17 are virtually identical to original claims 4 and 18, and thus the amendment amounted to no amendment at all. Applicant even canceled original claims 4 and 18 to avoid having duplicate claims present in the application.

If the current ground of rejection is more appropriate than that found in the first office action, then the Office should have given it in the first action, at least with respect to claims 4 and 18. MPEP §706.02 requires that a prior art rejection "be confined strictly to the best available art." In issuing a new ground of rejection for claims 1 and 17, the Office is conceding that it did not follow this requirement for original claims 4 and 18. Applicant's decision to move the limitations of claims 4 and 18 into the independent claims does not excuse this failure to apply the best available art to those claims.

In the end, the Office has not met its obligations under MPEP §706.02 and §707.06(a) and thus has issued an improper final action. Applicant asks the Office to remedy this error by issuing a new, non-final action now.

The Rejection Under - 35 U.S.C. § 112

Applicant disagrees with the Office in its interpretation of the term "void" but nevertheless has amended claim 20.

The 102(e) Rejection

Archambeault does not show or suggest a printed circuit board (PCB) having a lossy element that both connects electrically between the power and ground layers and resides on an internal layer of the PCB. Archambeault's Figure 4, showing RC circuit elements connected between power and ground, is not a cross-sectional diagram showing the physical placement of those elements – it is a schematic diagram showing an equivalent circuit. Archambeault says absolutely nothing about placing elements physically on internal layers of the PCB, and no one of ordinary skill in the art would confuse the schematic diagram of Figure 4 as a suggestion to place these elements physically on internal layers.

The 103(a) Rejection

Like Archambeault, none of secondary references (Klaser, Nakanishi, Ehman) shows a loss element residing in an internal PCB layer and connected electrically between power and ground to suppress electrical noise. Nakanishi does show embedded circuit elements, but these elements are not embedded among layers of a printed circuit board. Instead, they are components of hybrid multi-chip module (MCM). The materials, processes, structures and characteristics of the multi-chip module are radically different from those of the PCB, and no person of ordinary skill in the art of PCB fabrication would look to Nakanishi's MCM design for inspiration.

Moreover, the components embedded in Nakanishi's multi-chip module are not loss elements like that claimed, connected between power and ground to suppress electrical noise by introducing loss in the power loop. They are common circuit elements (termination resistors, voltage dividers, etc.) like those appearing in virtually all electronic circuits made over the last several decades. In short, nothing in the Nakanishi reference would suggest to a person of ordinary skill in the art that Archambeault's lossy caps should or even could reside in an internal PCB layer.

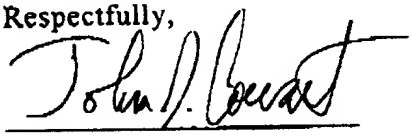
Ehman teaches how to place standard circuit components on internal layers of a PCB to conserve real estate and reduce cost. This in no way suggests Applicant's technique of introducing loss between power and ground to suppress unwanted electrical

noise and placing the loss element within the PCB to bring it closer to the power and ground layers.

CONCLUSION

Neither Archambeault by itself, nor Archambeault combined with Klaser, Ehman or Nahanishi, shows or suggests the features of Applicant's claims. All of the claims are therefore allowable over these references. Applicant asks the Examiner to reconsider this application and to allow all of the claims. Please apply any charges that might be due, except the issue fee, to deposit account 50-1673.

Respectfully,



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AMENDED CLAIMS

20. (Amended) A printed circuit board comprising multiple layers, including:

at least one layer on which electronic circuitry resides;

at least one power layer for use in providing electric current to the electronic circuitry, comprising:

[at least one void formed in the power layer; and]

at least one resistive element formed in a [the] void in the power layer and connected electrically to the power layer to suppress electrical noise created by sudden changes in current flow; and

at least one capacitive element connected in series with the resistive element.